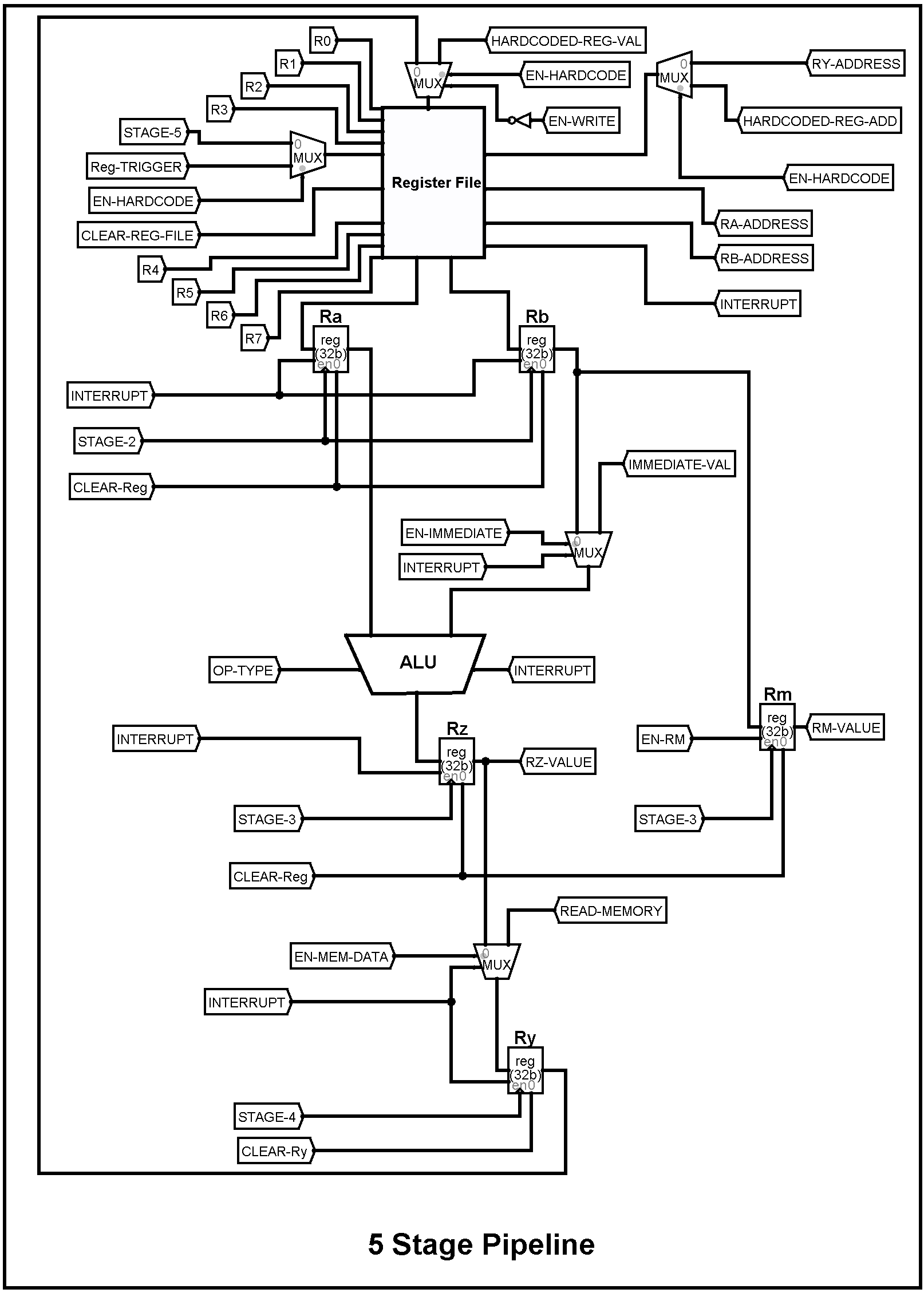
**Overall Architecture:**

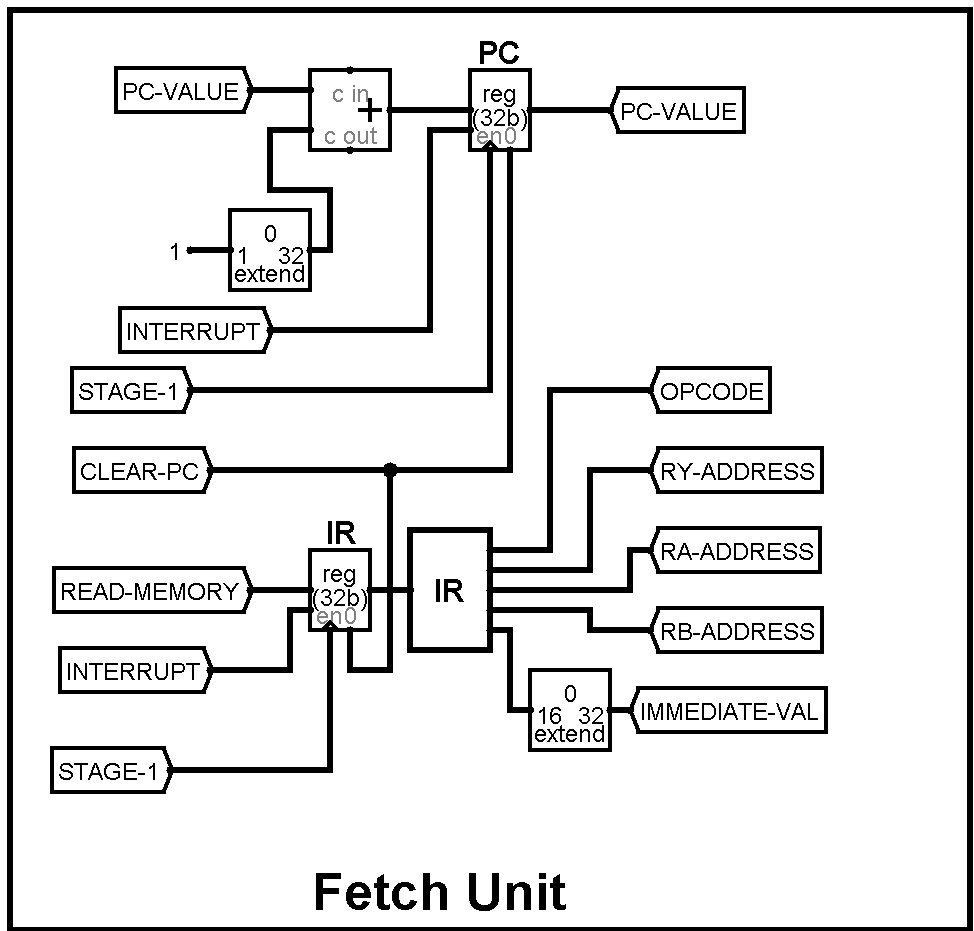
|  |  |
| --- | --- |
| **Components** | **Description** |
| General Purpose Registers (GPRs) | 8: R0 – R7 |
| Special Purpose Registers (SPRs) | 7: PC, IR, RA, RB, RZ, RM, RY |
| Memory | RAM: 8 – bit Address Line and 32 – bit Data |
| Instruction Supported | 13 |

**Components:**

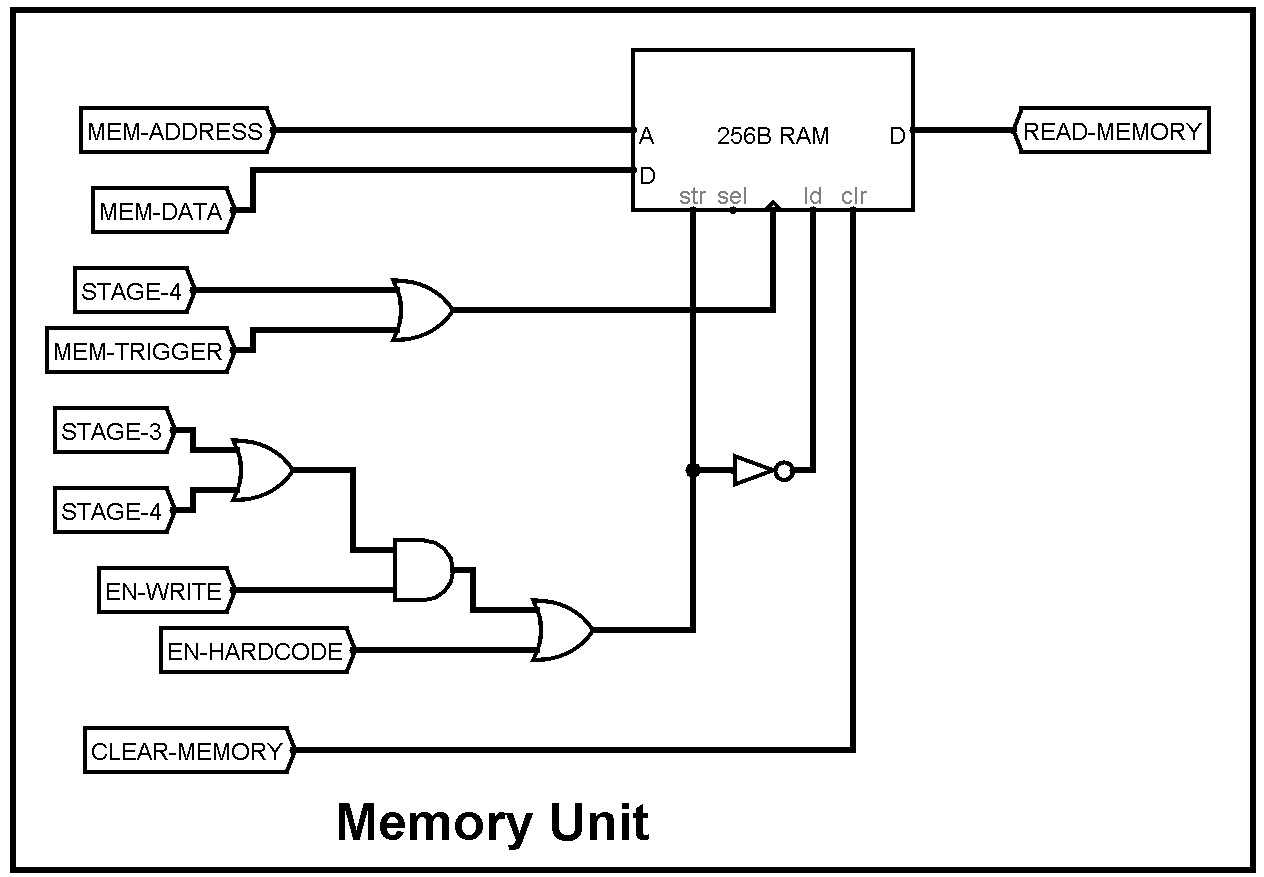
1. Processor Pipeline – 5 stage pipeline



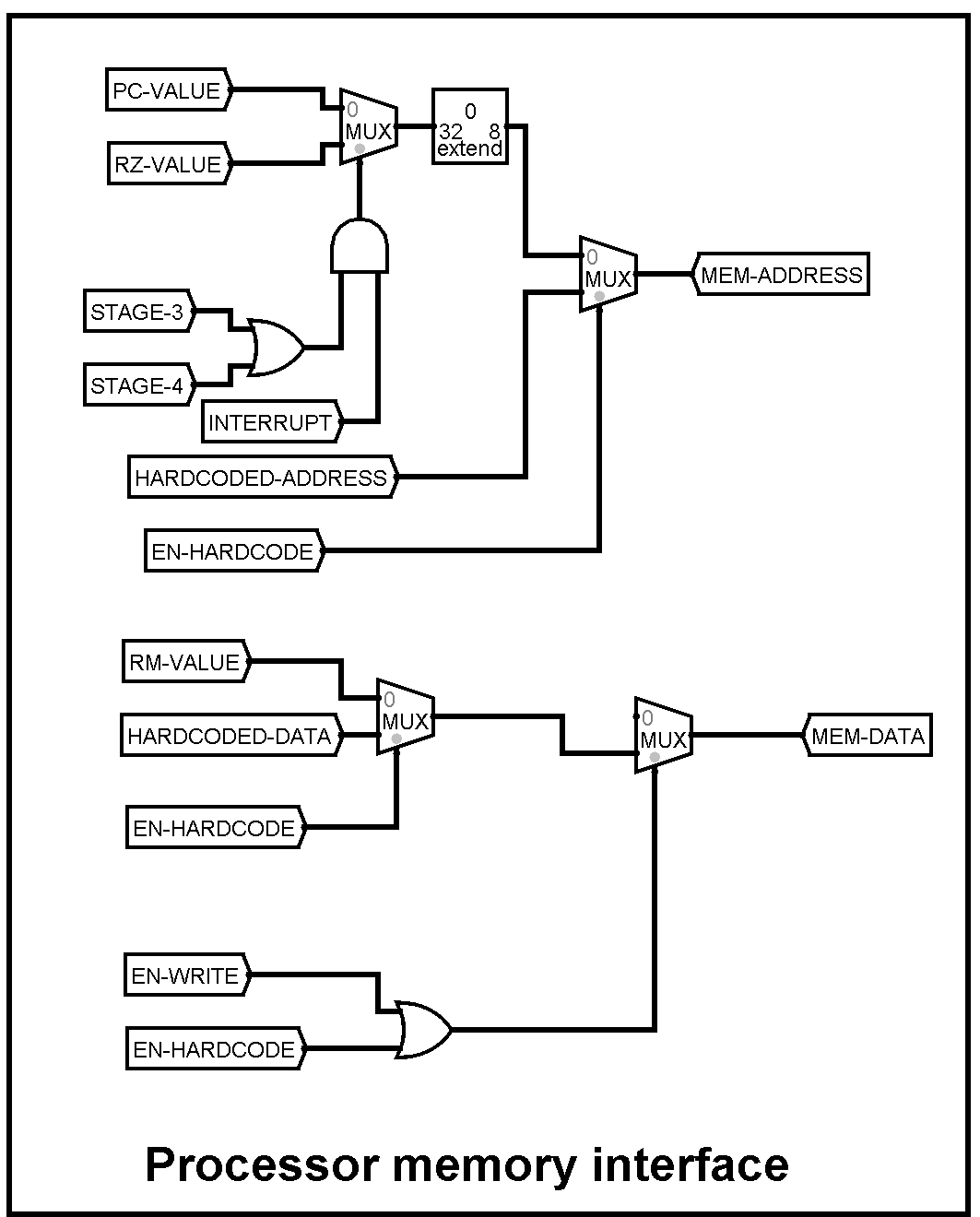
1. Fetch Unit



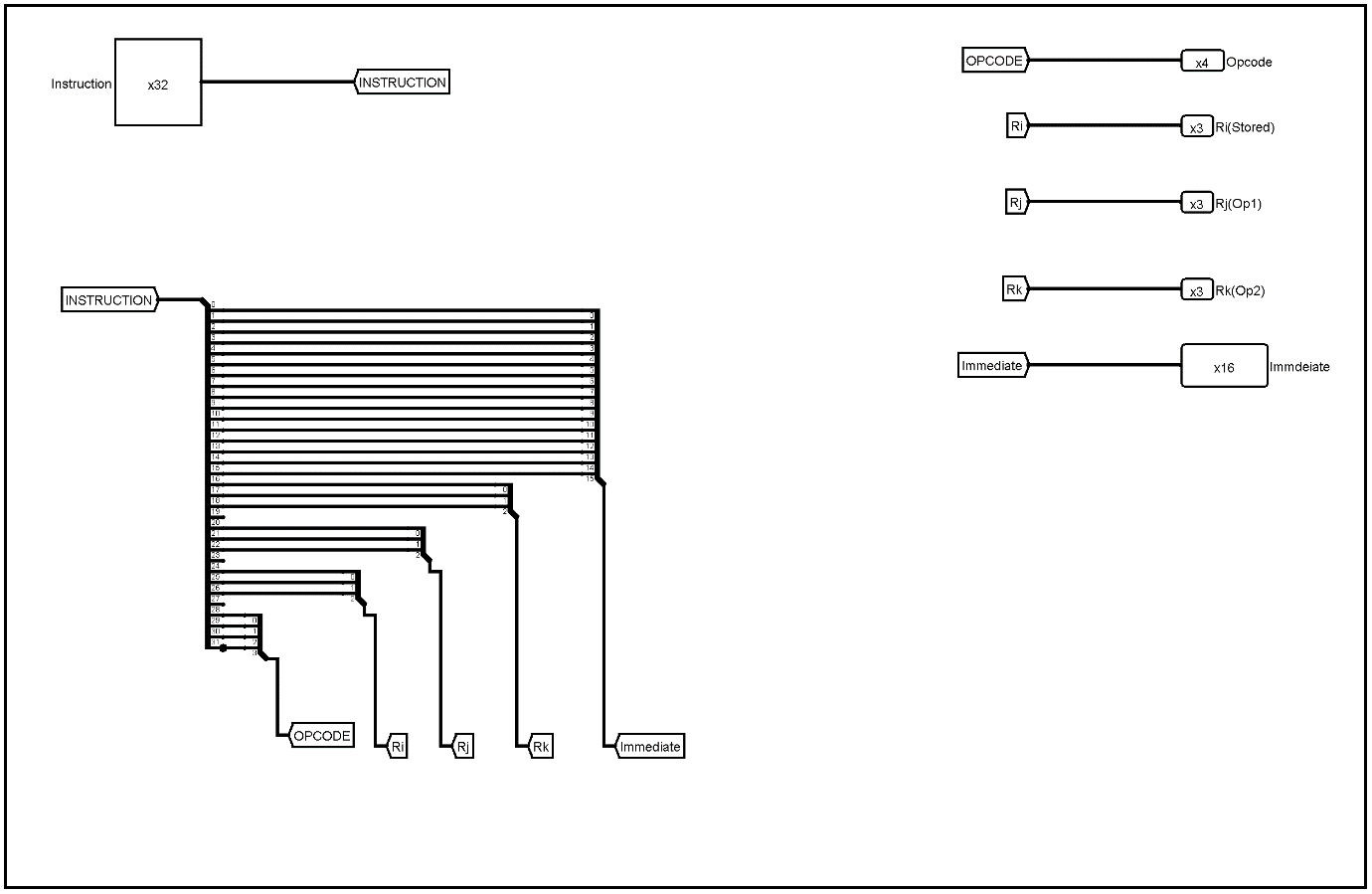
1. Memory Unit



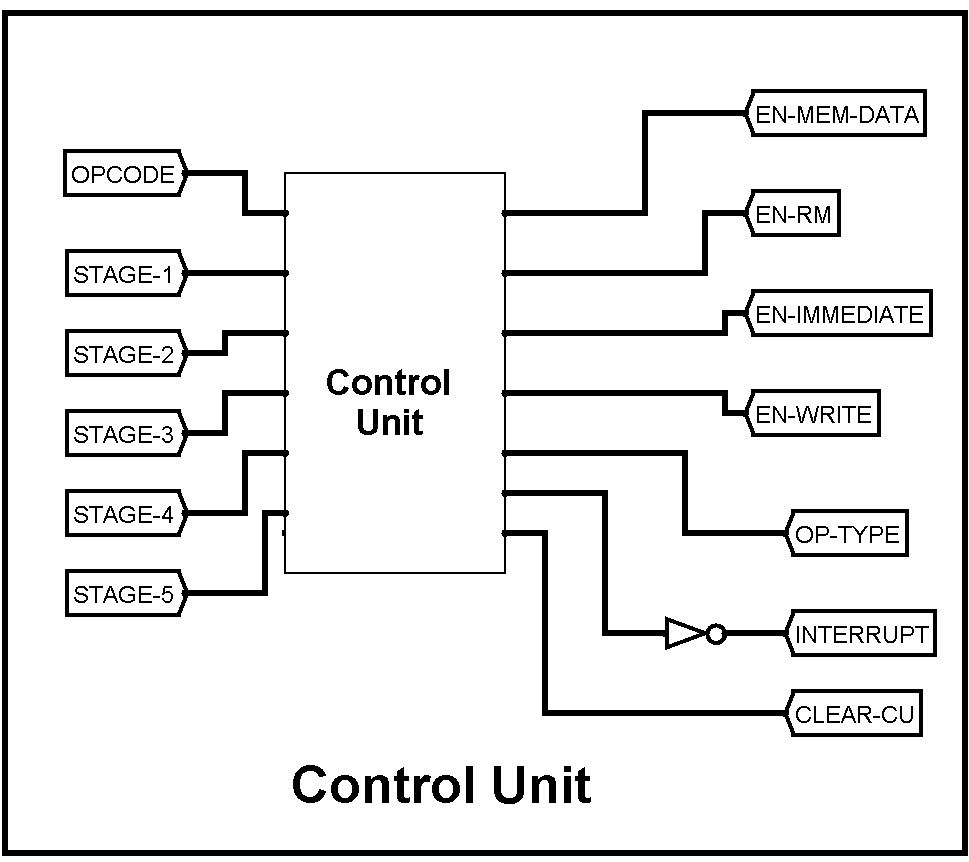
1. Processor Memory Interface

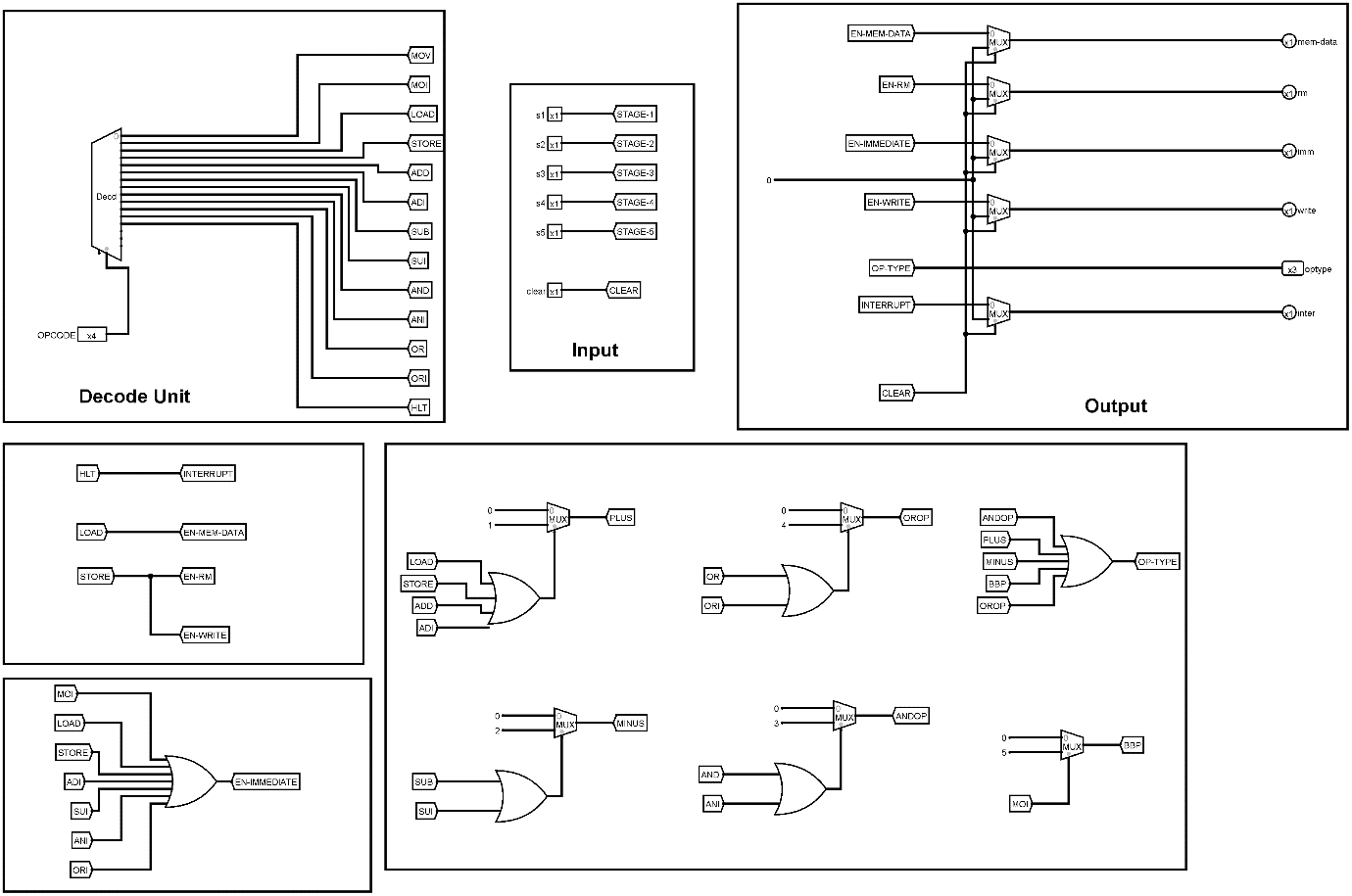


1. Instruction Register – internal circuit

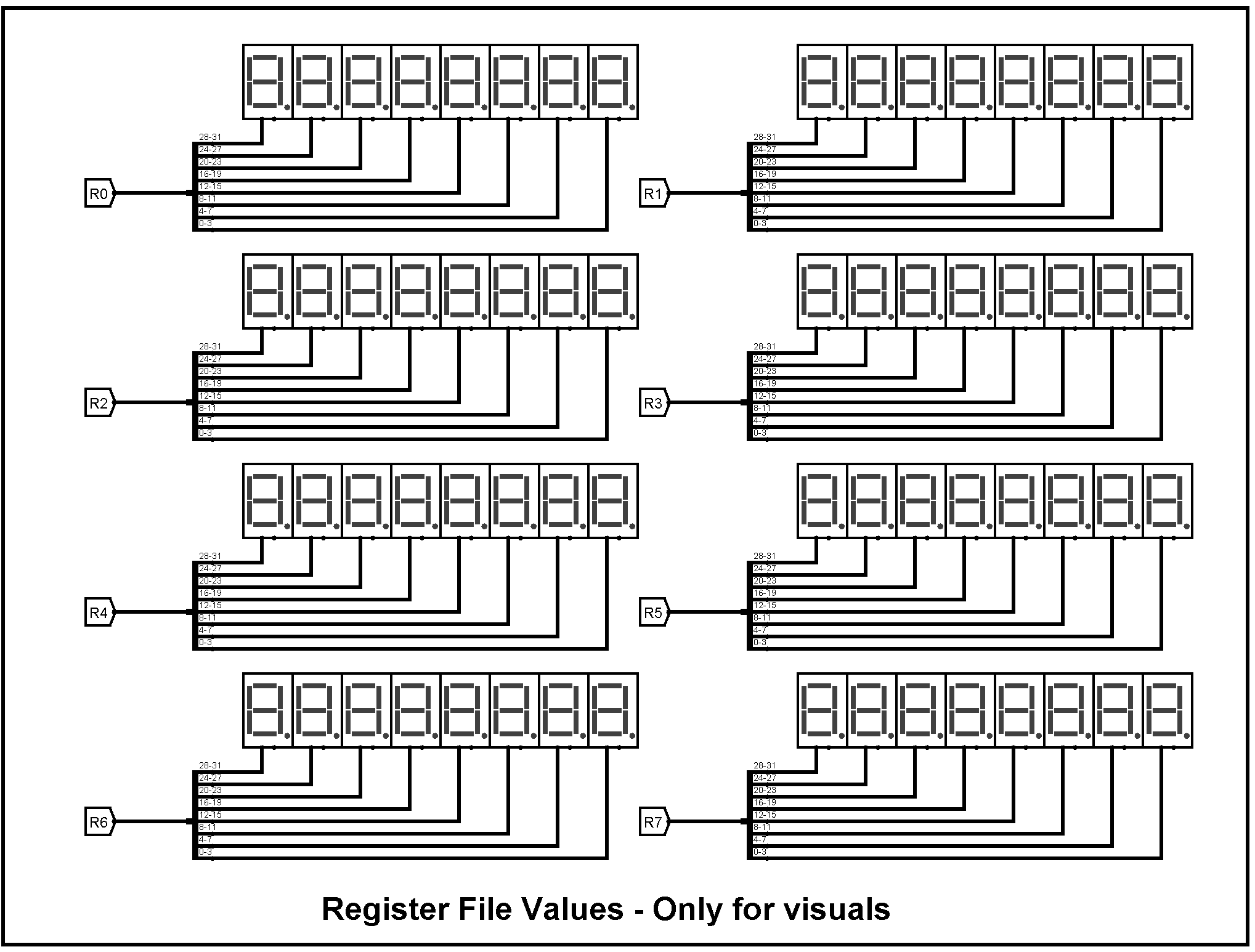


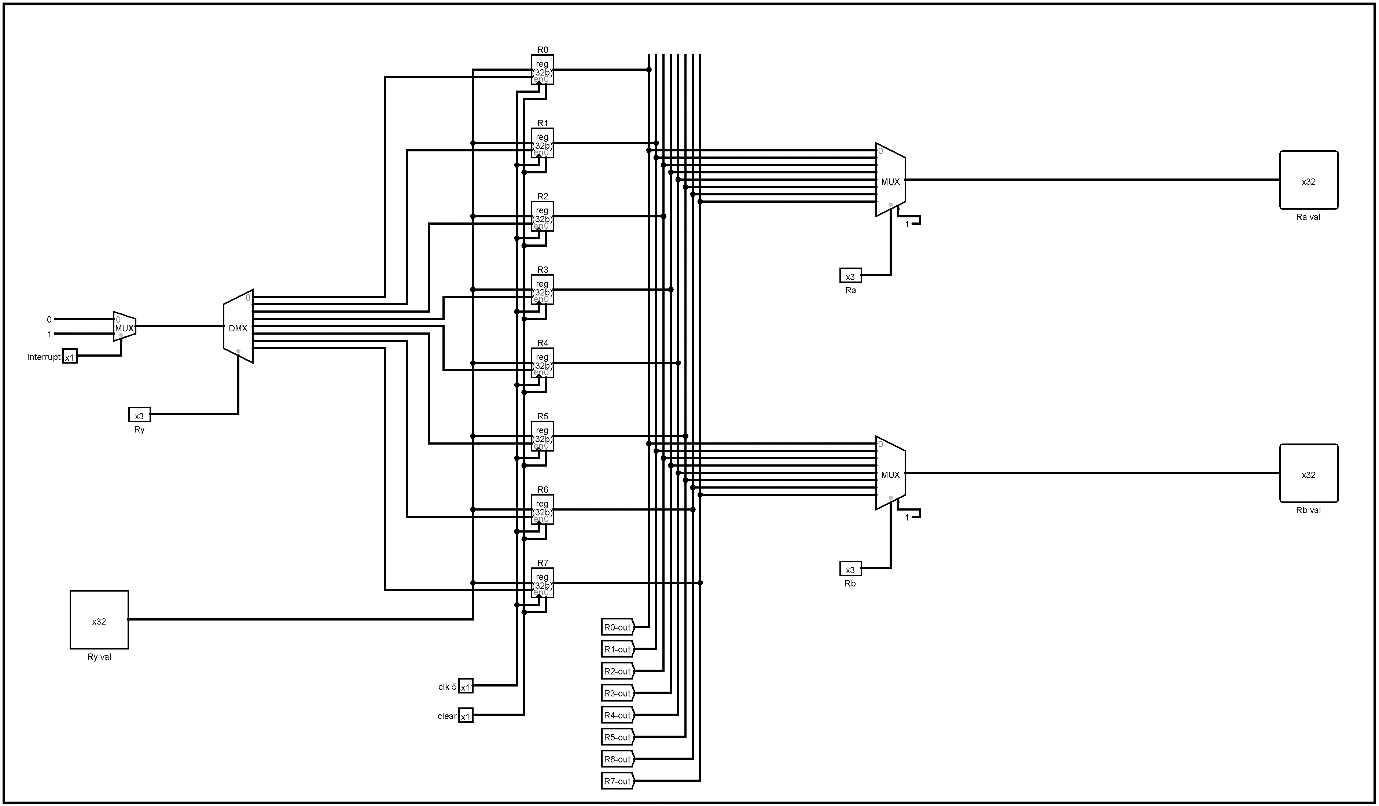
1. Control Unit



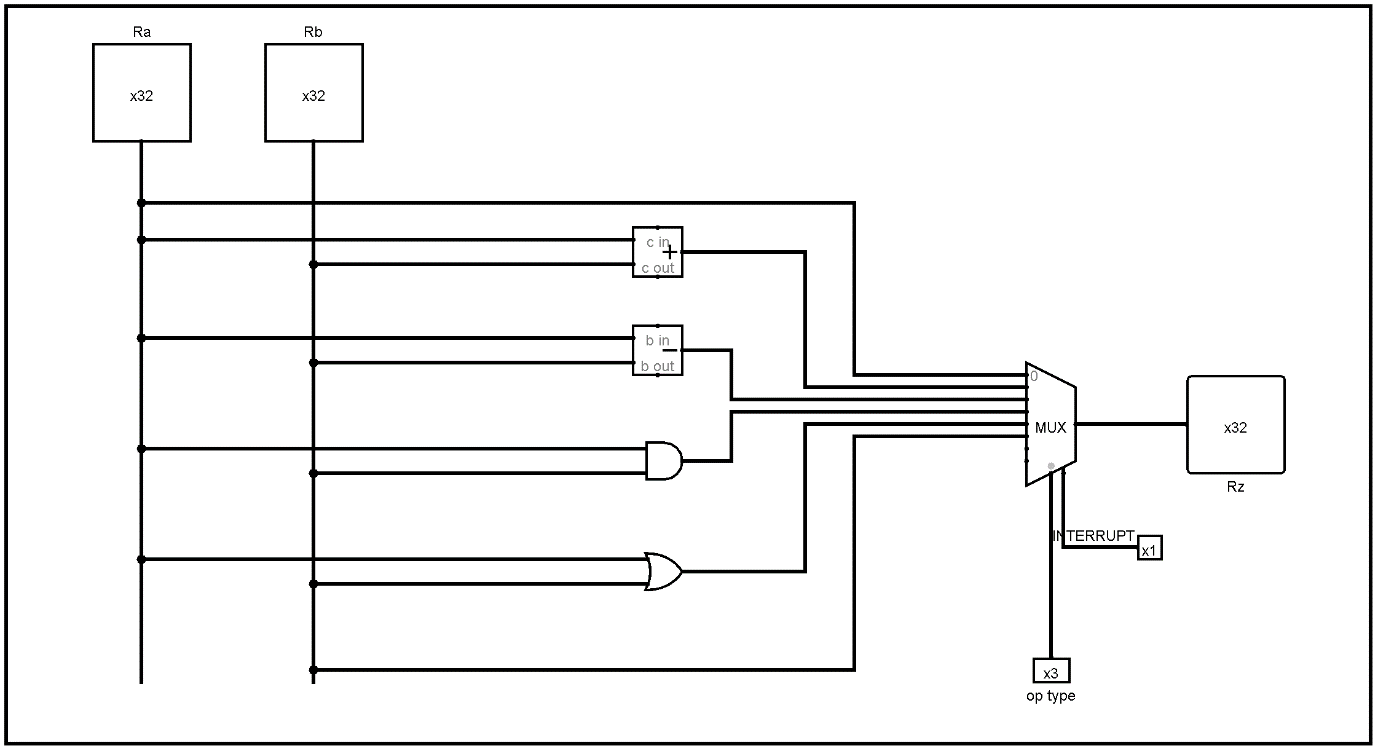


1. Register File





1. ALU – Internal circuit



1. Stage Counter

